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MAIL STOP APPEAL BRIEF
PATENT
8017-1105

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Taro FUJII et al. Appeal No. _____

Application No. 10/694,822 Group 2183

Filed October 29, 2003 Examiner B. Johnson

ARRAY-TYPE PROCESSOR HAVING PLURAL PROCESSOR ELEMENTS CONTROLLED BY A STATE CONTROL UNIT

APPEAL BRIEF

MAY IT PLEASE YOUR HONORS:

(i) **Real Party in Interest**

The real party in interest in this appeal is the assignee, NEC Electronics Corporation of Kanagawa, Japan.

(ii) **Related Appeals and Interferences**

None.

(iii) **Status of Claims**

Claims 1, 9, 15 and 21-35 are pending. This appeal is taken from the final rejection of claims 9, 15 and 21-35. Claim 1 is allowed. Claims 2-8, 10-14 and 16-20 were previously canceled.

(iv) **Status of Amendments**

No amendment was filed subsequent to the final rejection of the claims on appeal.

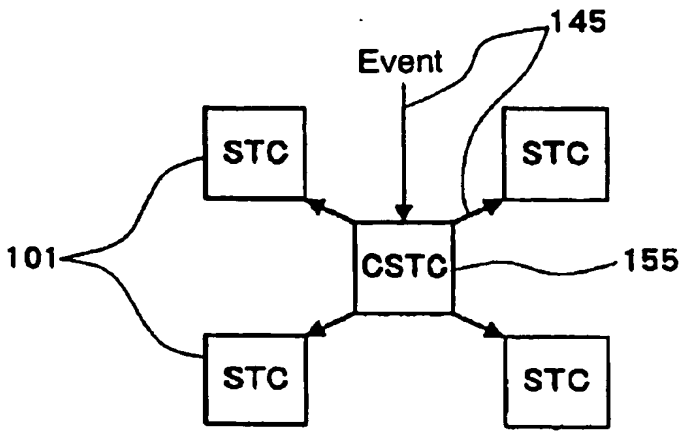
(v) **Summary of Claimed Subject Matter**

Each of independent claims 9, 15 and 21 is directed to an array-type processor in which a multiplicity of processor elements is arranged in rows and columns. Operation of the multiplicity of processor elements is controlled by a state control unit (see specification page 1, lines 4-9).

Claim 9 recites that an array-type processor includes a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns (see page 4, lines 18-23). The array-type processor also includes a plurality of state control units that intercommunicate to realize linked operation as necessary (see page 4, line 25 to page 5, line 1). The array-type processor further includes an event distributing means for distributing said event data to said plurality of state control units (see Figure 7, page 5, lines 1-2 and page 13, lines 12-16).

As illustrated by way of example in Figure 13, reproduced below, claim 9 further recites that a central control unit 155 distributes said event data to said plurality of state control units 101 (see page 21, lines 22-25). The central control unit 155 is surrounded by said plurality of state control units 101 and is connected by said event distributing means to all of said plurality of state control units (see page 21, lines 22-23).

Fig. 13



Claim 9 still further recites that the instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data (see page 4, lines 23-25 and page 10, lines 11-15). The event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit (see page 5, lines 8-11).

Claim 15 differs from claim 9 by further specifying the relationship between the state control units, the plurality of processor elements and the event distributing means, and by omitting the claim 9 requirement that the central control unit is surrounded by the plurality of state control units and is

connected by said event distributing means to all of said plurality of state control units.

Claim 15 recites the following features of claim 9:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns. Page 4, lines 18-23.

a plurality of state control units that intercommunicate to realize linked operation as necessary. Page 4, line 25 to page 5, line 1.

an event distributing means for distributing said event data to said plurality of state control units. Page 5, lines 1-2.

the instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with the event data. Page 4, lines 23-25 and page 10, lines 11-15.

said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit. Page 5, lines 8-11.

The features of claim 15 that are different from claim 9 are that the multiplicity of processor elements <u>is divided into</u>

element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements (see Figure 3 and page 7, line 17 to page 8, line 6), that each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas (see page 7, lines 22-24), and that said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units (page 13, lines 17-19).

Claim 21 differs from claim 9 by further specifying the relationship between the number of state control units and the plurality of processor elements, and by omitting the claim 9 requirement that the central control unit is surrounded by the plurality of state control units and is connected by said event distributing means to all of said plurality of state control units. Claim 21 also omits the claim 9 definition of event data, which is found on page 5, lines 8-11.

Claim 21 recites the following features of claim 9:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns. Page 4, lines 18-23.

a plurality of state control units that intercommunicate to realize linked operation as necessary. Page 4, line 25 to page 5, line 1.

an event distributing means for distributing said event data to said plurality of state control units. Page 5, lines 1-2.

The features of claim 21 that are different from claim 9 are that a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit (page 10, lines 11-16) and in which state transitions of said multiplicity of processors elements are done while changing a configuration of said multiplicity of processor elements (page 10, lines 18-25).

Claim 21 further differs from claim 9 by requiring that transitions of said operating states are done by said state control unit in accordance with a computer program that has been installed in advance and event data which are supplied by said multiplicity of processor elements (see page 4, lines 23-25 and page 10, lines 11-15), that the multiplicity of said processor elements is divided among a number of element areas corresponding to the number of said plurality of state control units, said number of element areas being less than said multiplicity of processor elements, said element areas being separate areas of said array-type processor that each have a plurality of processor elements, and that each of said plurality of state control units is connected to said processor elements corresponding to each of

said plurality of state control units within respective element areas.

(vi) **Grounds of Rejection to be Reviewed on Appeal**

The first issue on appeal is whether claim 9 would have been obvious, in the meaning of 35 USC §103(a), based on KATSUKI et al. US 5,581,767 in view of common art.

The second issue on appeal is whether claims 15, 21, 23-25, 30, 32, 33 and 35 would have been obvious, in the meaning of 35 USC §103(a), based on KATSUKI in view of STOKES et al. US 3,537,074.

The third issue on appeal is whether claims 22, 26-29, 31 and 34 would have been obvious, in the meaning of 35 USC §103(a), based on KATSUKI in view of STOKES and further in view of MAY et al. US 6,414,368.

(vii) **Argument**

First Issue on Appeal

Claim 9 would not have been obvious based on KATSUKI in view of common art.

Figure 2 is exemplary of KATSUKI and shows a host computer 58 (offered as a control unit) connected by buses 48, 50 and 56 (offered as event distributing means) to a plurality of controllers 22 (offered as state control units).

The final rejection recognizes that KATSUKI fails to disclose a central control unit surrounded by plural state control units (see page 10, last two lines).

The final rejection concludes that Figure 2 of KATSUKI is a schematic drawing that is not meant to limit the configuration of KATSUKI and that it would have been obvious to modify KATSUKI to minimize the wire distance and overall size of the device (see page 11).

However, even if one of ordinary skill in the art were to consider the proposed modification, the invention of claim 9 would not result.

Claim 9 specifies that a central control unit distributes said event data to said plurality of state control units. The central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units.

A configuration as recited in claim 9 centralizes the data for uniform distribution (see page 21, line 22 to page 22, line 9).

KATSUKI teaches away from a configuration in which there is uniform distribution in favor of a dual bus structure with first and second bus structures that are different from each other. Column 7, lines 24-64 describe an exemplary bus structure of KATSUKI wherein the first bus structure transfers data for two

immediately adjacent processor units and the second bus structure for processor units that are beyond the third nearest ones in order to provide a flexible data transfer.

Thus, even if the host computer 58 as seen in Figure 2 of KATSUKI, which is offered as a central control unit, were moved to a central location as suggested in the final rejection, such modification would not result in a uniform distribution as KATSUKI requires two different bus structures.

It is clear that KATSUKI is based on a bus structure with immediately adjacent elements and elements that are not immediately adjacent. KATSUKI uses a first bus structure for the immediately adjacent elements and a different second bus structure for the elements that are not immediately adjacent. See claims 1 and 14. KATSUKI does not suggest a structure other than what is explicitly shown in Figure 2.

Moreover, KATSUKI could not be modified to meet the present claims. Modifying KATSUKI in the manner suggested to have a central control unit surrounded by a plurality of processors would require all the bus structures to be the same, which would change the basic principle under which KATSUKI was designed to operate, that is having two different bus structures, one for immediately adjacent elements and another for elements that are not immediately adjacent. As one of ordinary skill in the art would not be motivated to change the principle of operation of

KATSUKI, the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Second Issue on Appeal

Claims 15, 21, 23-25, 30, 32, 33 and 35 would not have been obvious based on KATSUKI in view of STOKES.

A number of the claims are argued separately using the headings below.

Claim 15

Claim 15 recites among other features a multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements.

KATSUKI describes a bus structure that acts to form pairs of processor units and control/memory units in a one-to-one correspondence (see column 6, lines 10-12 and lines 32-34).

STOKES discloses four control units each directly coupled to and controlling a respective processor array (plural processors). See column 3, line 73 to column 4, line 1.

The final rejection concludes on page 12 that: "The fact that KATSUKI mentions a one-to-one correspondence several times within the patent disclosure does not mean that it would not have been obvious to change this aspect."

However, this position is contrary to one of the basic theories underlying *prima facie* obviousness, i.e., the suggested

combination cannot change the basic principle under which the primary reference was designed to operate.

In the present case, KATSUKI does not just mention a one-to-one correspondence a few times, but rather, restricts the invention to such an embodiment.

At column 5, lines 32-37, KATSUKI discloses: "This invention is embodied in a bus structure ... comprising a processor ... and a control/memory section ... corresponding one-to-one to the aforementioned processor". Column 7, lines 53-56 discloses that the one-to-one correspondence accomplishes an efficient data transfer.

Further, each of the claims of KATSUKI recites a one-to-one correspondence between a plurality of control/memory units and a plurality of processor units.

In view of the above, it is believed to be apparent that the entire disclosure of KATSUKI is explicitly limited to and thus, based on the basic principle of operation of a one-to-one correspondence between a control unit and a processor.

Modifying KATSUKI in the manner suggested to have a single control unit for a plurality of processors would change the principle of operation of KATSUKI. As one of ordinary skill in the art would not be motivated to change the principle of operation of KATSUKI, the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Claim 21

Claim 21 includes a similar feature to that of claim 15 and recites that the multiplicity of processor elements is divided into a number of element areas corresponding to the number of state control units. The number of element areas being less than the multiplicity of processor elements.

As set forth above, KATSUKI clearly requires a one-to-one correspondence between processor units and control units.

The conclusion in the final rejection that KATSUKI discloses other than a one-to-one relationship between element areas/state control units and processor elements is incorrect.

Moreover, claim 21 recites that a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit.

Such switching the context of each operation cycle involves switching (changing) the configuration of the data paths (of the multiplicity of processor elements). In the recited array processor, the context is switched not only by the computer program, but also by the event data.

In contrast, it is apparent that KATSUKI is directed to a bus architecture, which requires a bus protocol. KATSUKI is incapable of propagating the event data for each operation cycle, since KATSUKI requires operating on bus protocol. The bus

protocol of KATSUKI is a combination of a first bus for adjacent processors and a second bus for long-distance ones.

In view of the above, it is apparent that KATSUKI operates on a different premise than that which is recited. Accordingly, there is no factual support for the conclusion that it would have been obvious to one of ordinary skill in the art to modify KATSUKI to meet the recited configuration.

Third Issue on Appeal

Claims 22, 26-29, 31 and 34 would not have been obvious based on KATSUKI in view of STOKES and further in view of MAY.

MAY is directed to a microcomputer having communication links arranged to provide non-shared connections to similar links of other microcomputers. MAY does not overcome the shortcomings of KATSUKI and STOKES set forth above with respect to claim 21. Since claims 22, 26-29, 31 and 34 depend from claim 21 and further define the invention, claims 22, 26-29, 31 and 34 are believed to be patentable at least for depending from an allowable independent claim.

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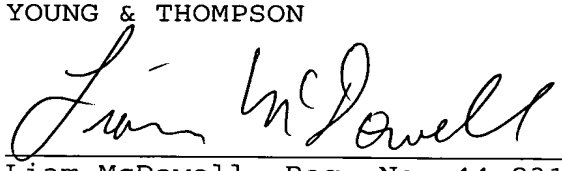
Conclusion

Appellants respectfully urge that the rejections on appeal should not be maintained, and respectfully request that these rejections be reversed.

Respectfully submitted,

YOUNG & THOMPSON



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(viii) **Claims Appendix**

1. An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary; and

an event distributing means for distributing said event data to said plurality of state control units, said event distributing means comprising dedicated event communication lines that connect said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data, and

wherein said plurality of state control units comprises at least four state control units that are directly interconnected to each other by respective dedicated event communication lines so that each of said at least four state control units is directly connected to all other ones of said state control units.

9. An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary;

an event distributing means for distributing said event data to said plurality of state control units; and

a central control unit for distributing said event data to said plurality of state control units, said central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data,

wherein said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit.

15. An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary; and

an event distributing means for distributing said event data to said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data,

wherein said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements,

wherein each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas, and

wherein said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units, said event data are data for causing a

transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit.

21. An array-type processor in which a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes for which data is individually set, are arranged in rows and columns; and in which a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit; and in which state transitions of said multiplicity of processors elements are done while changing a configuration of said multiplicity of processor elements, wherein:

transitions of said operating states are done by said state control unit in accordance with a computer program that has been installed in advance and event data which are supplied by said multiplicity of processor elements;

said state control unit is composed of a plurality of units that intercommunicate to realize linked operation as necessary;

the multiplicity of said processor elements is divided among a number of element areas corresponding to the number of said plurality of state control units, said number of element areas being less than said multiplicity of processor elements,

said element areas being separate areas of said array-type processor that each have a plurality of processor elements;

each of said plurality of state control units is connected to said processor elements corresponding to each of said plurality of state control units within respective element areas; and

said array-type processor includes an event distributing means for distributing said event data to said plurality of state control units that intercommunicate and realize linked operation.

22. An array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication lines that connect said plurality of state control units.

23. An array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication buses that connect said plurality of state control units.

24. An array-type processor according to claim 21, wherein:

data buses for transmitting processing data of said plurality of processor elements are arranged in matrix form;

a plurality of switch elements, which switch-control a wiring configuration of said data buses in accordance with

instruction codes that are individually set as data, are arranged in matrix form together with said processor elements;

said state control units successively switch said instruction codes of said plurality of processor elements and said plurality of switch elements; and

said event distributing means is constituted by said data buses that are switch-controlled by said switch elements.

25. An array-type processor according to claim 22, wherein all of said plurality of state control units are interconnected by said event distributing means.

26. An array-type processor according to claim 22, wherein:

said plurality of state control units are arranged in rows and columns; and

said state control units are connected by said event distributing means to a portion of said state control units that are located in a vicinity.

27. An array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to state control units that are located in eight directions in the vicinity.

28. An array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to said state control units that are adjacent in four row and column directions.

29. An array-type processor according to claim 26, wherein a central control unit is provided for distributing said event data to said plurality of state control units; and said central control unit is connected by said event distributing means to all of said plurality of state control units.

30. An array-type processor according to claim 21, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means.

31. An array-type processor according to claim 26, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means.

32. An array-type processor according to claim 21, wherein one item of said event data that has been selected by said input selection means is supplied as output to said event distributing means.

33. An array-type processor according to claim 21, wherein output selection means is provided for each of said state control units, said output selection means selecting one from a plurality of items of said event data that are simultaneously received as input by said event distributing means and supplying these event data as output to said event distributing means.

34. An array-type processor according to claim 26, wherein:

said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.

35. An array-type processor according to claim 21, wherein:

said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.

(ix) **Evidence Appendix**

None.

(x) **Related Proceedings Appendix**

None.